



R6500 Microcomputer System

DATA SHEET

CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The \overline{RES} input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

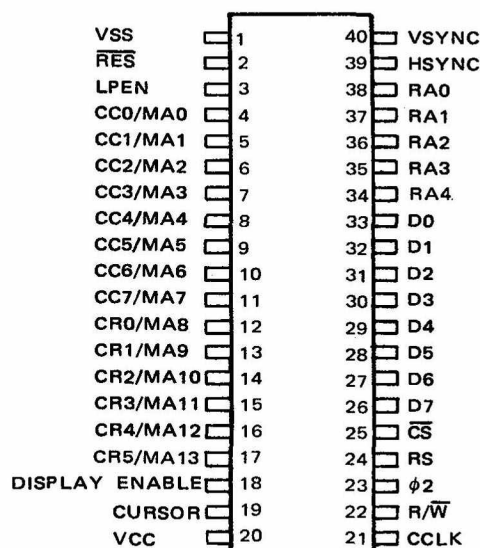
FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 \pm 5% Volt Power Supply

CRT CONTROLLER (CRTC)

ORDERING INFORMATION

Part Number	Package Type	Frequency	Temperature Range
R6545-1P	Plastic	1 MHz	0°C to +70°C
R6545-1AP	Plastic	2 MHz	0°C to +70°C
R6545-1C	Ceramic	1 MHz	0°C to +70°C
R6545-1AC	Ceramic	2 MHz	0°C to +70°C



R6545-1 Pin Configuration

INTERFACE SIGNAL DESCRIPTION

CPU INTERFACE

$\phi 2$ (Phase 2 Clock)

The input clock is the system Phase 2 ($\phi 2$) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable $\phi 2$ clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/\bar{W} (Read/Write)

The R/\bar{W} input signal generated by the processor is used to control the direction of data transfers. A high on the R/\bar{W} pin allows the processor to read the data supplied by the R6545-1, a low on the R/\bar{W} pin allows data on data lines D0-D7 to be written into the R6545-1.

\bar{CS} (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when \bar{CS} is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/\bar{W} = low) into the Address Register and reads (R/\bar{W} = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected (\bar{CS} = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

\bar{RES}

The \bar{RES} signal is an active-low input used to initialize all internal scan counter circuits. When \bar{RES} is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. \bar{RES} must stay low for at least one CCLK period. All scan timing is initiated when \bar{RES} goes high. In this way, \bar{RES} can be used to synchronize display frame timing with line frequency. \bar{RES} may also be used to synchronize multiple CRTCs in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

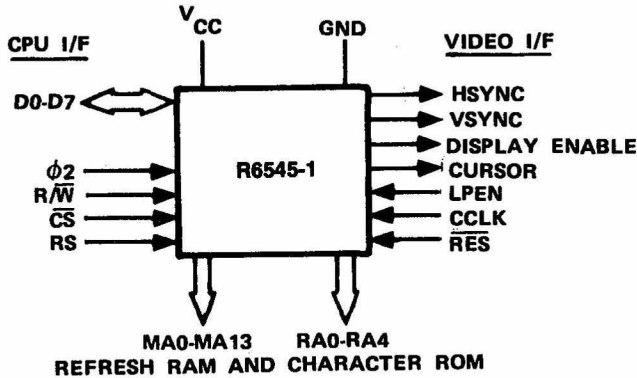
RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

INTERNAL REGISTER ORGANIZATION

CS	RS	Address Register					Reg. No.	Register Name	Register Units	Read (R/W = High)	Write (R/W = Low)	Register Bit							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X												
0	0	X	X	X	X	X	X	Address Register	Register No.		✓								
0	0	X	X	X	X	X	X	Status Register	—	✓									
0	1	0	0	0	0	0	R0	Horizontal Total Char	No. of Characters/Row		✓								
0	1	0	0	0	0	1	R1	Horizontal Displayed Char	No. of Characters/Row		✓								
0	1	0	0	0	1	0	R2	Horizontal Sync Position	Character Position		✓								
0	1	0	0	0	1	1	R3	YSYNC, HSYNC Widths	No. of Scan Lines, Characters		✓								
0	1	0	0	1	0	0	R4	Vertical Total Rows	No. of Character Rows		✓								
0	1	0	0	1	0	1	R5	Vertical Total Adjust Lines	No. of Scan Lines		✓								
0	1	0	0	1	1	0	R6	Vertical Displayed Rows	No. of Character Rows		✓								
0	1	0	0	1	1	1	R7	Vertical Sync Position	No. of Character Rows		✓								
0	1	0	1	0	0	0	R8	Mode Control	—		✓								
0	1	0	1	0	0	1	R9	Scan Line	No. of Scan Lines		✓								
0	1	0	1	0	1	0	R10	Cursor Start Line	Scan Line No.		✓								
0	1	0	1	0	1	1	R11	Cursor End Line	Scan Line No.		✓								
0	1	0	1	1	0	0	R12	Display Start Address (H)	—		✓								
0	1	0	1	1	0	1	R13	Display Start Address (L)	—		✓								
0	1	0	1	1	1	0	R14	Cursor Position Address (H)	—	✓	✓								
0	1	0	1	1	1	1	R15	Cursor Position Address (L)	—	✓	✓								
0	1	1	0	0	0	0	R16	Light Pen Register (H)	—	✓									
0	1	1	0	0	0	1	R17	Light Pen Register (L)	—	✓									

Table 1. Overall Register Structure and Addressing



R6545-1 Interface Diagram

INTERNAL REGISTER DESCRIPTION

ADDRESS REGISTER

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. Its contents is the number of the desired register (0-17). When CS and RS are low, then this register may be loaded; when CS is low and RS is high, then the register selected is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

This 8-bit register contains the status of the CRTC. Only two bits are assigned, as follows:

7	6	5	4	3	2	1	0
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
—	LRF	VRT	—	—	—	—	—

NOT USED

Vertical Re-Trace (VRT)

0 = Scan is not currently in its vertical re-trace time.
1 = Scan is currently in its vertical re-trace time.

Note that this bit actually goes to a "1" when vertical re-trace starts, but goes to a "0" five character clock times before vertical re-trace ends, so that critical timings for refresh RAM operations are avoided.

LPEN Register Full (LRF)

0 = Register R16 or R17 has been read by the CPU.

1 = LPEN strobe has been received.

Not Used

NOTE: The Status Register takes the State,

—	0	1	—	—	—	—	—
---	---	---	---	---	---	---	---

immediately after power (V_{CC}) turn-on.

R0—HORIZONTAL TOTAL CHARACTERS

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

R1—HORIZONTAL DISPLAYED CHARACTERS

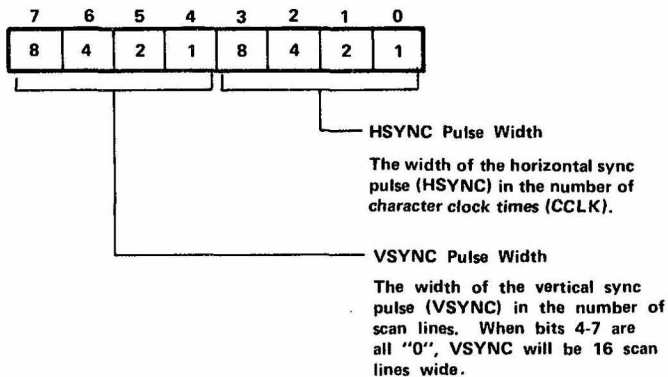
This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

This 8-bit write-only register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the R6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then \overline{RES} may be used to provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

The Vertical Total Line Adjust Register (R5) is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

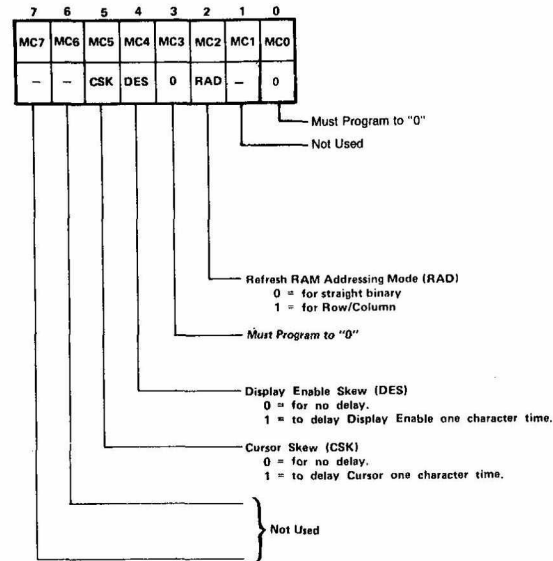
This 7-bit write-only register contains the number of displayed character rows in each frame.

R7—VERTICAL SYNC POSITION

This 7-bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:



R9—ROW SCAN LINES

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE

R11—CURSOR END LINE

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

Bit 6	Bit 5	Cursor Blink Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

R12—DISPLAY START ADDRESS HIGH

R13—DISPLAY START ADDRESS LOW

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

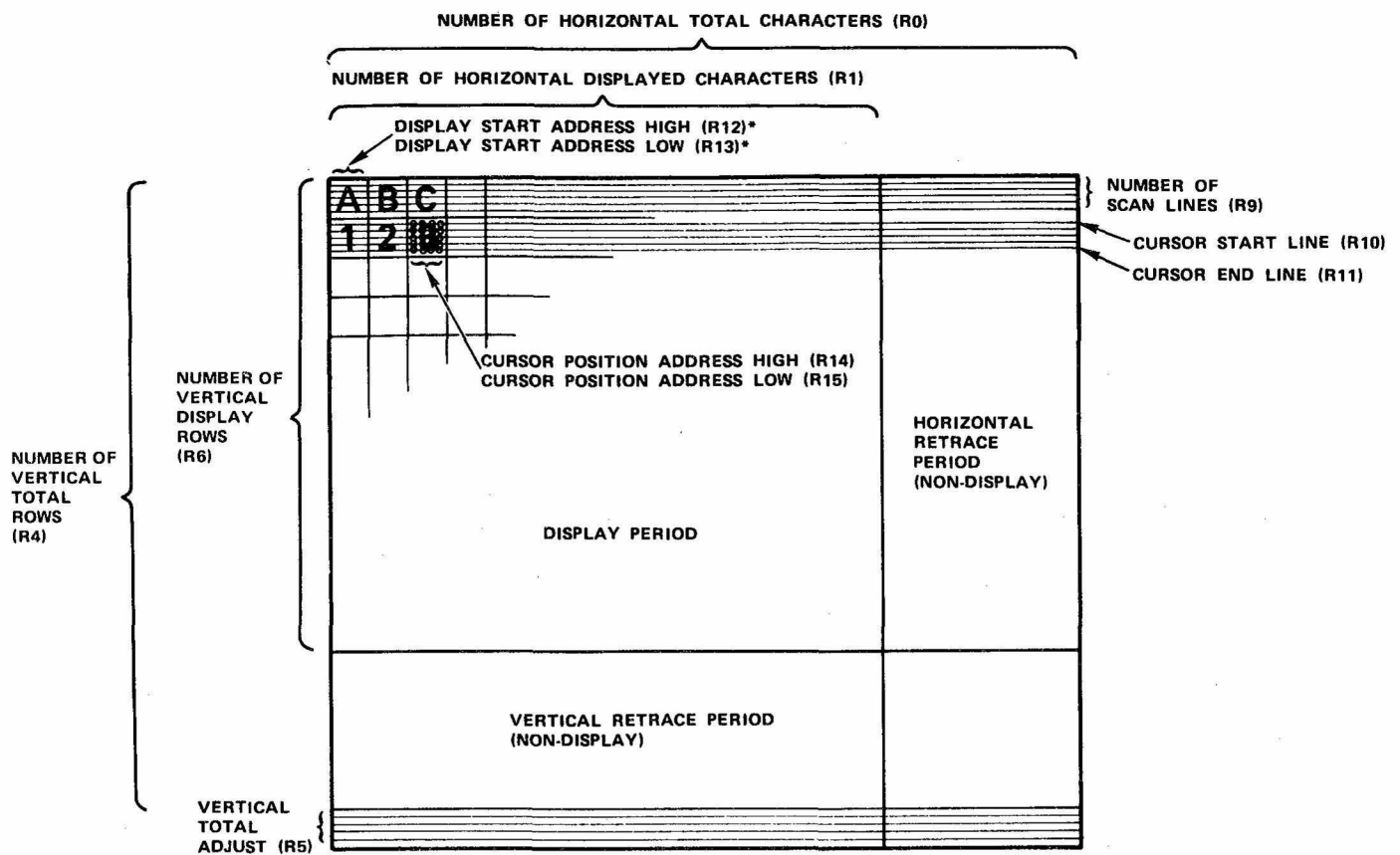


Figure 1. Video Display Format

R14—CURSOR POSITION HIGH R15—CURSOR POSITION LOW

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

R16—LIGHT PEN HIGH R17—LIGHT PEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

- (1) Straight binary, if register R8, bit 2 = "0".
- (2) Row/Column, if register R8, bit 2 = "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 1 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are used for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and are used to trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

Shared Memory Mode (R8, bit 3 = "0")

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

ADDRESSING MODES

Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits the use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 2 illustrates Refresh RAM addressing for the case of binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

TOTAL = 90											
DISPLAY = 80											
TOTAL = 34 DISPLAY = 24	0	1	2	3	76	77	78	79	80	81	89
	80	81	82	83	156	157	158	159	160	161	169
	160	161	162			237	238	239	240		249
	240	241	242			317	318	319	320		329
	1680	1681	1682			1757	1758	1759	1760		1769
	1760	1761	1762			1837	1838	1839	1840		1849
	1840	1841	1842			1917	1918	1919	1920		1929
	1920	1921	1922			1997	1998	1999	2000		2009
	2000	2001	2002			2077	2078	2079	2080		2089
	2640	2641	2642			2717	2718	2720			2729

Figure 2. Memory Addressing Example (80 x 24)

CURSOR OPERATION

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

Bits 5 and 6 in the Cursor Start Line High Register (R10) control the cursor display and blink rate as follows:

Bit 6	Bit 5	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

The cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

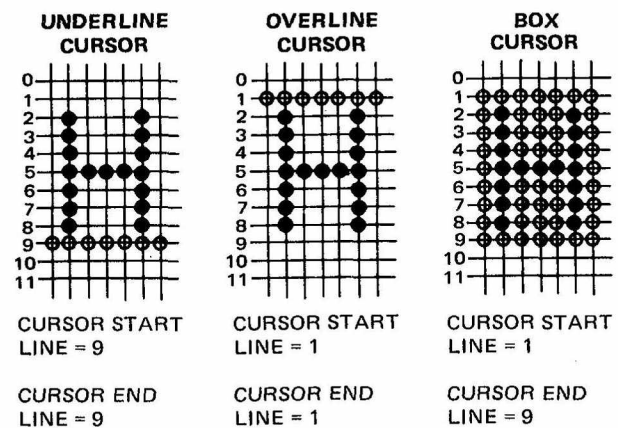


Figure 3. Cursor Display Scan Line Control Examples

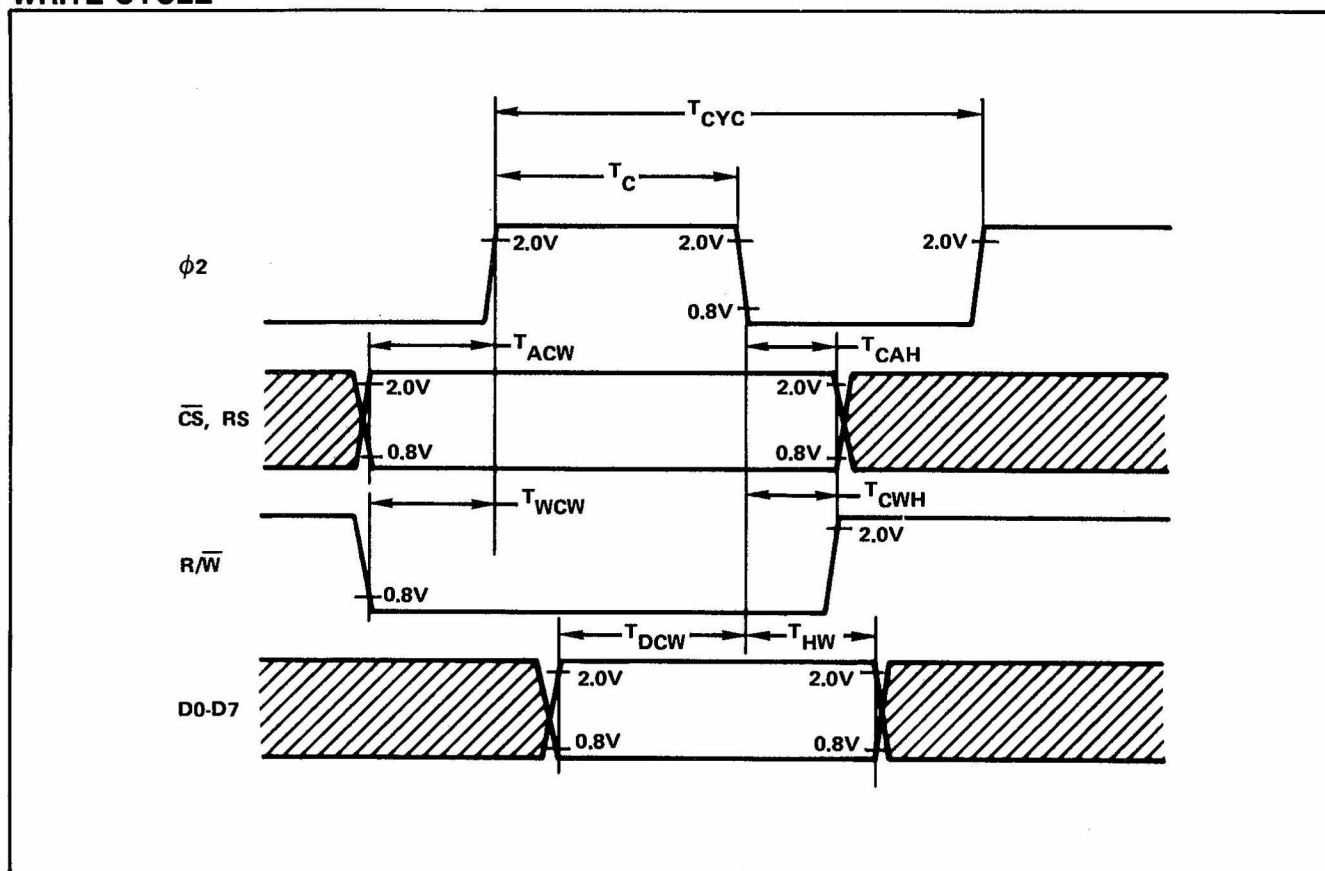
MPU WRITE TIMING CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^{\circ}C$, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	—	0.5	—	μs
$\phi 2$ Pulse Width	T_C	440	—	200	—	ns
Address Set-Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAH}	0	—	0	—	ns
R/\overline{W} Set-Up Time	T_{WCW}	180	—	90	—	ns
R/\overline{W} Hold Time	T_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	265	—	100	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns

(t_r and $t_f = 10$ to 30 ns)

WRITE CYCLE



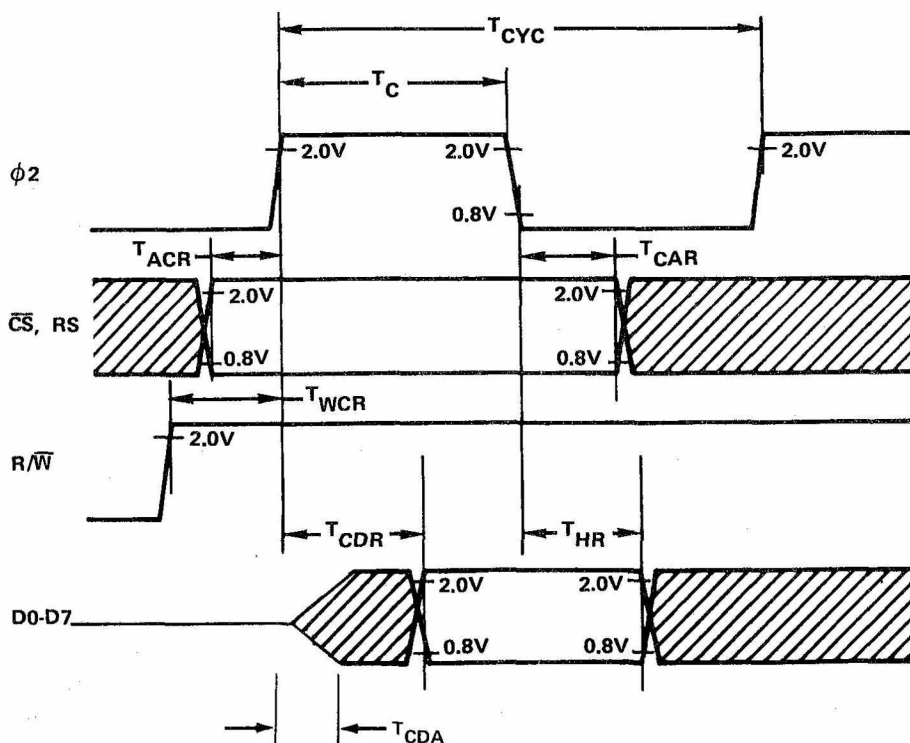
MPU READ TIMING CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^{\circ}C$, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	—	0.5	—	μs
$\phi 2$ Pulse Width	T_C	440	—	200	—	ns
Address Set-Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
R/\overline{W} Set-Up Time	T_{WCR}	180	—	90	—	ns
Read Access Time	T_{CDR}	—	340	—	150	ns
Read Hold Time	T_{HR}	10	—	10	—	ns
Data Bus Active Time (Invalid Data)	T_{CDA}	40	—	40	—	ns

(t_r and $t_f = 10$ to 30 ns)

READ CYCLE



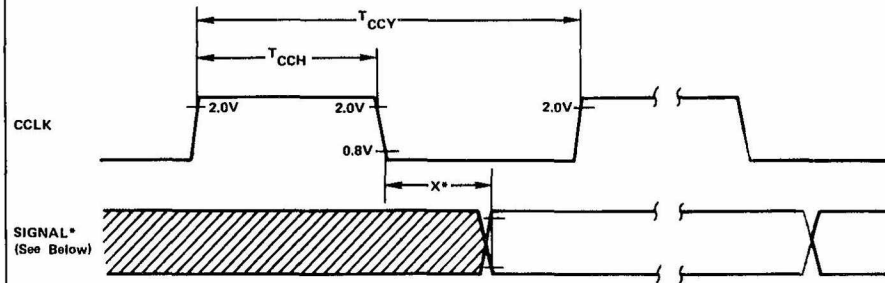
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $T_A = 0$ to $70^\circ C$, unless otherwise noted)

Characteristics	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Char. Clock Cycle Time	T_{CCY}	0.4	40	0.4	40	μs
Char. Clock Pulse Width	T_{CCH}	200	—	200	—	ns
MA0-MA13 Propagation Delay	T_{MAD}	—	300	—	300	ns
RA0-RA4 Propagation Delay	T_{RAD}	—	300	—	300	ns
DISPLAY ENABLE Prop. Delay	T_{DTD}	—	450	—	450	ns
HYSYNC Propagation Delay	T_{HSD}	—	450	—	450	ns
VSYNC Propagation	T_{VSD}	—	450	—	450	ns
Cursor Propagation Delay	T_{CDD}	—	450	—	450	ns
LPEN Strobe Width	T_{LPH}	150	—	150	—	ns
LPEN to CCLK Delay	T_{LP1}	20	—	20	—	ns
CCLK to LPEN Delay	T_{LP2}	0	—	0	—	ns

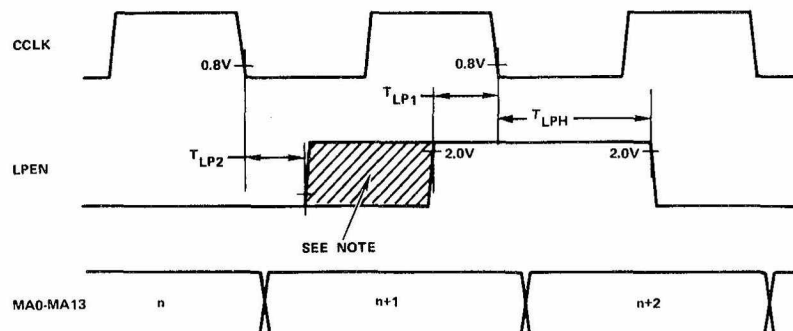
$t_r, t_f = 20$ ns (max)

SYSTEM TIMING DEFINITIONS



SIGNAL	SIGNAL SYMBOL (X)
MA0-MA13	T_{MAD}
RA0-RA4	T_{RAD}
DISPLAY ENABLE	T_{DTD}
HYSYNC	T_{HSD}
VSYNC	T_{VSD}
CURSOR	T_{CDD}

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:

SLASH AREA DEFINES THE "WINDOW" IN WHICH AN LPEN POSITIVE EDGE WILL CAUSE ADDRESS N+2 TO LOAD INTO LIGHT PEN REGISTER. TRANSITIONS ON EITHER SIDE OF THIS "WINDOW" WILL RESULT IN UNPREDICTABLE VALUES BEING LOADED INTO THE LIGHT PEN REGISTER.

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

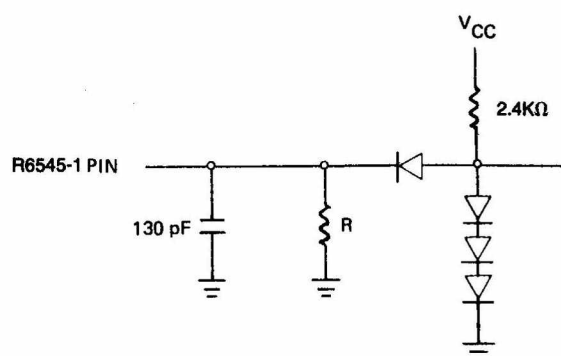
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be taken to prevent unnecessary application of voltages in excess of the allowable limits.

Electrical Characteristics

($V_{CC} = 5.0V \pm 5\%$, $T_A = 0-70^\circ C$, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0.3	0.8	Vdc
Input Leakage ($\overline{\text{Q2}}$, $\overline{\text{R/W}}$, $\overline{\text{RES}}$, $\overline{\text{CS}}$, RS, LPEN, CCLK)	I_{IN}	—	2.5	μAdc
Three-State Input Leakage (D0-D7) ($V_{IN} = 0.4$ to $2.4V$)	I_{TSI}	—	10.0	μAdc
Output High Voltage $I_{LOAD} = 205 \mu\text{Adc}$ (D0-D7) $I_{LOAD} = 100 \mu\text{Adc}$ (all others)	V_{OH}	2.4	—	Vdc
Output Low Voltage $I_{LOAD} = 1.6 \text{ mAdc}$	V_{OL}	—	0.4	Vdc
Power Dissipation	P_D	—	1000	mW
Input Capacitance $\overline{\text{Q2}}$, $\overline{\text{R/W}}$, $\overline{\text{RES}}$, $\overline{\text{CS}}$, RS, LPEN, CCLK	C_{IN}	—	10.0	pF
D0-D7		—	12.5	pF
Output Capacitance	C_{OUT}	—	10.0	pF

TEST LOAD



R=11KΩ FOR D0-D7
=24KΩ FOR ALL OTHER OUTPUTS