commodore INFORMATION

APPLICATIONS BRIEF #5

DUAL PROCESSOR CONFIGURATION WITH THE MPS 6508

The MPS 6508 has been designed with a non-overlapping two phase clock. The potential behind this may not be apparent until one examines a control line that is available on the 6508 - the AEC . What this means to the user is the power to design a dual processor system capable of running at full speed with virtually no overhead.

The AEC line can be used to tri-state the address bus. Since data is valid only during phase two high, with minimal logic, it will be possible for two 6508s to access common memory on opposite phase of the same clock.

Figure 1 shows a simple block diagram connecting two processors together. The timings are illustrated in Figure 2.

FIGURE 1

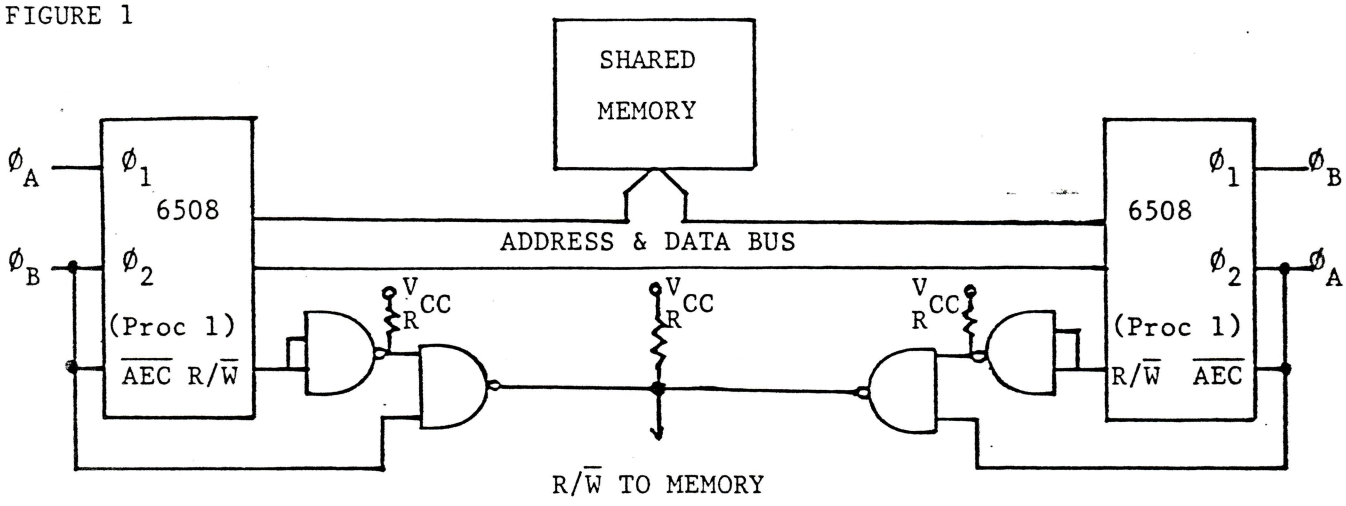
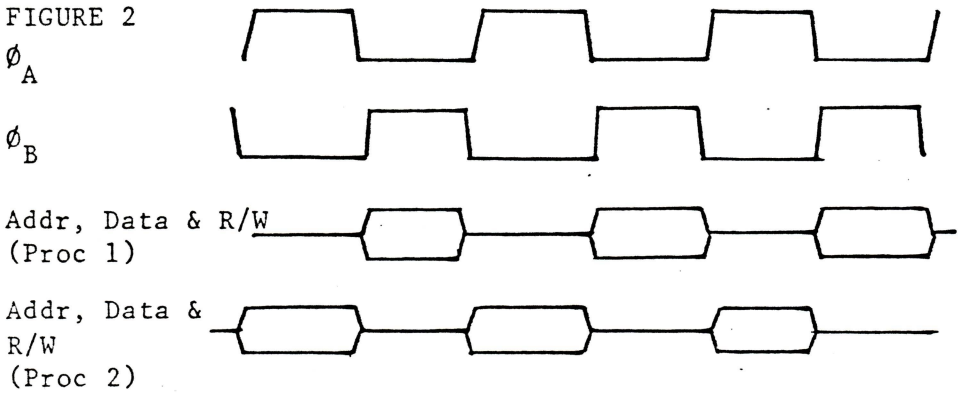


FIGURE 2



Note: Open Collector NAND Gates (7401) used for R/$\overline{W}$ Signal.